

**What Is Claimed Is:**

1           1.    A receiver circuit for outputting signals to an  
2           internal circuit supplied with a first power supply voltage,  
3           comprising:

4                a reference voltage circuit supplied with the first power  
5                supply voltage for outputting a reference voltage  
6                that is a mid-point voltage between the first power  
7                supply voltage and ground;

8                a reference current circuit for generating a first current  
9                according to the reference voltage; and

10              a receiving circuit supplied with a second power supply  
11              voltage higher than the first power supply voltage,  
12              comprising:

13                a first current source for generating a second  
14                current according to the first current; and

15                a differential amplifier circuit for generating an  
16                output signal contained within a voltage range  
17                of the first power supply voltage and centered  
18                around the mid-point voltage to the internal  
19                circuit according to the second current.

1           2.    The receiver circuit as claimed in claim 1, wherein  
2           the internal circuit comprises a plurality of transistors having  
3           a first gate oxide thickness.

1           3.    The receiver circuit as claimed in claim 2, wherein  
2           the reference voltage circuit comprises a first PMOS transistor  
3           and a first NMOS transistor having the first gate oxide  
4           thickness.

1           4.     The receiver circuit as claimed in claim 3, wherein  
2     the first PMOS transistor and the first NMOS transistor have a  
3     first p/n ratio.

1           5.     The receiver circuit as claimed in claim 4, wherein  
2     the transistors of the internal circuit have the first p/n ratio.

1           6.     The receiver circuit as claimed in claim 3, wherein  
2     the first PMOS transistor and the first NMOS transistor are  
3     connected in serial and between the first power supply voltage  
4     and ground, and the gates and the drains of the first PMOS  
5     transistor and the first NMOS transistor are connected.

1           7.     The receiver circuit as claimed in claim 4, wherein  
2     the reference current circuit comprises:

3           a comparator circuit having a reverse input terminal, a  
4           non-reverse input terminal coupled to the gates of  
5           the first PMOS transistor and the first NMOS  
6           transistor, and an output terminal;

7           a first resistor coupled between the reverse input terminal  
8           and ground; and

9           a second current source coupled between the second power  
10          supply voltage and the first resistor for generating  
11          the first current flowing through the first resistor  
12          and generating the mid-point voltage at the  
13          connection point of the first resistor and the  
14          reverse input terminal.

1           8.     The receiver circuit as claimed in claim 1, wherein  
2     the second current is referenced to the first current by a  
3     current mirror or equivalent circuitry.

1           9.    The receiver circuit as claimed in claim 7, wherein  
2 the differential amplifier circuit comprises:

3           a second PMOS transistor having a first source coupled to  
4           the second current source, a first gate coupled to  
5           an I/O signal, and a first drain;

6           a third PMOS transistor having a second source coupled to  
7           the second current source, a second gate coupled to  
8           a reverse I/O signal, and a second drain;

9           a second resistor coupled between the connection point of  
10          the first drain and the internal circuit, and ground;  
11          and

12          a third resistor coupled between the connection point of  
13          the second drain and the internal circuit, and  
14          ground.

1           10.   The receiver circuit as claimed in claim 7, wherein  
2 the second and third PMOS transistors have a second gate oxide  
3 thickness larger than the first gate oxide thickness.

1           11.   The receiver circuit as claimed in claim 9, wherein  
2 the resistances of the second and third resistor are the same.

1           12.   The receiver circuit as claimed in claim 1, wherein  
2 the mid-point voltage is approximately a switching point voltage  
3 of the internal circuit.

1           13.   A receiver circuit, comprising:

2           an internal circuit supplied with a first power supply  
3           voltage and comprising a plurality of transistors  
4           having a first p/n ratio and a first gate oxide  
5           thickness;

6 a reference voltage circuit supplied with the first power  
7 supply voltage and comprising a first PMOS transistor  
8 and a first NMOS transistor having a first p/n ratio  
9 and the first gate oxide thickness, for outputting  
10 a reference voltage that is a mid-point voltage  
11 between the first power supply voltage and ground;  
12 a reference current circuit for generating a first current  
13 according to the reference voltage; and  
14 a receiving circuit supplied with a second power supply  
15 voltage higher than the first power supply voltage,  
16 comprising:  
17 a first current source for generating a second  
18 current according to the first current; and  
19 a differential amplifier circuit for generating an  
20 output signal contained within a voltage range  
21 of the first power supply voltage and centered  
22 around the mid-point voltage to the internal  
23 circuit according to the second current.

1 14. The receiver circuit as claimed in claim 13, wherein  
2 the first PMOS transistor and the first NMOS transistor are  
3 connected in serial and between the first power supply voltage  
4 and ground, and the gates and the drains of the first PMOS  
5 transistor and the first NMOS transistor are connected.

1 15. The receiver circuit as claimed in claim 13, wherein  
2 the reference current circuit comprises:  
3 a comparator circuit having a reverse input terminal, a  
4 non-reverse input terminal coupled to the gates of

5           the first PMOS transistor and the first NMOS  
6           transistor, and an output terminal;  
7           a first resistor coupled between the reverse input terminal  
8           and ground; and  
9           a second current source coupled between the second power  
10          supply voltage and the first resistor for generating  
11          the first current flowing through the first resistor  
12          and generating the mid-point voltage at the  
13          connection point of the first resistor and the  
14          reverse input terminal.

1          16. The receiver circuit as claimed in claim 13, wherein  
2          the second current is referenced to the first current by a  
3          current mirror or equivalent circuitry.

1          17. The receiver circuit as claimed in claim 15, wherein  
2          the differential amplifier circuit comprises:

3           a second PMOS transistor having a first source coupled to  
4           the second current source, a first gate coupled to  
5           an I/O signal, and a first drain;

6           a third PMOS transistor having a second source coupled to  
7           the second current source, a second gate coupled to  
8           a reverse I/O signal, and a second drain;

9           a second resistor coupled between the connection point of  
10          the first drain and the internal circuit, and ground;  
11          and

12          a third resistor coupled between the connection point of  
13          the second drain and the internal circuit, and  
14          ground.

1           18. The receiver circuit as claimed in claim 17, wherein  
2 the second and third PMOS transistors have a second gate oxide  
3 thickness larger than the first gate oxide thickness.

1           19. The receiver circuit as claimed in claim 17, wherein  
2 the resistances of the second and third resistor are the same.

1           20. The receiver circuit as claimed in claim 13, wherein  
2 the mid-point voltage is approximately a switching point voltage  
3 of the internal circuit.